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[METHOD OF REDUCING PATTERN PITCH IN INTEGRATED CIRCUITS]

Abstract

A method of reducing pattern pitch is provided. A material layer, a hard mask layer and a patterned photoresist layer are sequentially formed over a substrate. Using the patterned photoresist layer as etching mask, the hard mask layer is etched. Due to the trenching effect, a residual hard mask layer remains in an exposed region exposed by the photoresist layer and micro-trenches are formed at the edges of the residual hard mask layer. Thereafter, using the residual hard mask layer as etching mask to pattern the material layer. Finally, the patterned photoresist layer and the hard mask layer are removed. In the invention, the trenching effect is utilized when etching the hard mask layer. A portion of the hard mask layer remains, and the micro-trenches are formed in the hard mask layer. After the micro-trenches are transferred to the material layer, the pattern pitch can be reduced.